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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ART UNIT	PAPER NUMBER
2133	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/368,918	TRABER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *19 August 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to amended claims 1 and 15 and previously examined claims 2-10 and 16-21 filed March 13, 2003 have been fully considered but they are not persuasive.

The Applicant contends, "Applicants respectfully submit that the Li reference does not teach or suggest an assertion or deassertion notification when logical values of a trigger signal are captured to begin a scan test enable signal assertion or deassertion as claimed in the present application. Moreover, the Li reference fails to teach or suggest a staging component for issuing a scan test enable signal based upon notification from a scan test enable trigger sensing component".

The Examiner asserts that Li teaches an automatic scan test enable signal assertion system (Delay Circuit 54 in Figures 3, 4A and 4B in the Li patent is an automatic scan test enable signal assertion system) comprising:

a scan test enable trigger sensing component (OR gate 94 in Figure 4B is a scan test enable trigger sensing component) for providing an assertion or deassertion notification (the output of the scan test enable trigger sensing component OR gate 94 provides a scan mode signal which is a logical signal provided to place scan elements into active or inactive to trigger the scan elements, hence the scan mode signal is an assertion or deassertion notification, see Abstract in Li) when logical values of a trigger signal

captured at multiple stages provide an indication to begin a scan test enable signal assertion or deassertion (the scan mode signal used to trigger the scan test is captered at flip-flop stages 98 and 100 in Figure 4B of Li prior to being provided to the scan test enable trigger sensing component OR gate 94); and

a staging component coupled to said scan test enable trigger sensing component (master-slave flip-flops 91 in Figure 4B are a staging component coupled to said scan test enable trigger sensing component OR gate 94), said staging component for advancing said logical values of said trigger signal through a plurality of stages in accordance with a progression signal (a clock signal required for any and every flip-flop for advancing signals through stages of flip-flops is a progression signal) and issuing an asserted or deasserted scan test enable signal based upon said assertion or deassertion notification (MUX San Enable Signal in Figure 204 shows that either an asserted or deasserted scan test enable signal is issued to various MUXs based upon said assertion or deassertion notification issued from the scan test enable trigger sensing component OR gate 94, also see Abstract, Li) from said scan test enable trigger sensing component.

In response to applicant's argument that "Li teaches away from the present invention by indicating scan enable signals are received from a scan mode pad", a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the

intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

The Examiner asserts that there is no structural difference between the invention claimed by the Applicants claim 1 and the circuit taught in Figure 3, 4A and 4B of Li and further more the fact that a scan test enable signal at the pad is used as an initial trigger to for Delay Circuit 54 in Figures 3, 4A and 4B in the Li patent does not change the fact that the scan test enable signal at the pad is still a trigger signal (since it is used to trigger the scan test) used by the Delay Circuit 54 to produce a MUX San mode signal for activating or deactivating the test.

The Applicant contends, "Moreover, the Li reference fails to teach or suggest utilizing a normal functional pin to communicate the trigger signal". The Examiner asserts that scan mode pads are normally used for scan testing hence are normal functional pads.

The Applicant contends, "Applicants respectfully assert that Li indicates that pad 50 is utilized to communicate a scan test enable signal as an input [Col. 3, lines 58 through 59; Col. 4, lines 35 through 38; and Col. 4 lines 65 through 67] and not for communicating a trigger signal". The Examiner asserts that the scan mode signal at the pad is used to trigger a scan test hence by the dictionary definition of trigger (i.e., a

mechanism for initiating a process, see Webster's dictionary), the scan mode signal at the pad is a trigger signal for initiating a scan test.

The Applicant contends, "Applicants respectfully assert that the use of a reset signal on a pad, dedicated to a scan test enable signnal would not have been obvious. Applicants respectfully assert that Li reference and does not teach, suggest, nor rendered obvious the present claimed invention". The Examiner asserts that the scan mode signal at the pad is used to start and stop the scan test, which is precisely the purpose the reset signal in the Applicants claim 2, hence the reset signal in the Applicant's claim 1 is a scan enable signal identical to the scan enable signal at the pad in the Li patent.

The Applicant contends, "Applicants respectfully assert that the Li reference does not teach or render obvious maintaining an active scan mode signal status as claimed in the present application". Figure 5 shows that the scan mode enable signal has both active and inactive ranges hence Li teaches maintaining an active scan mode signal status.

The Applicant contends, "201 and 204 in Figure 5 of Li do not teach or render obvious a NAND boolean logic component as claimed in the present application". The Examiner asserts that NAND logic can be used to implement the OR logic circuit taught in Li, in fact, ((A NAND A) NAND (B NAND B)) = A OR B, hence OR logic is mathematically isomorphic to NAND logic and it would not only be obvious to use NAND logic in place of OR logic but it would be mathematically trivial.

The Examiner disagrees with the applicant and maintains all rejections of amended claims 1 and 15 and previously examined claims 2-10 and 16-21. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that amended claims 1 and 15 and previously examined claims 2-10 and 16-21 are not patentably distinct or non-obvious over the prior art of record in view of the reference, Li, Hehching Harry (US 6023778 A) as applied in the last office action, Paper No. 6. Therefore, the rejection of amended claims 1 and 15 and previously examined claims 2-10 and 16-21 is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3 and 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Li, Hehching Harry (US 6023778 A).

See Paper No. 6 for detailed action of prior rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 2, 4-10 and 19-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Li, Hehching Harry (US 6023778 A).

See Paper No. 6 for detailed action of prior rejections.

4. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li, Hehching Harry (US 6023778 A) In view of Jin, London (US 6114892 A).

35 U.S.C. 103(a) rejection of claim 11.

Li teaches scan test enable signal activation system (Delay Circuit 54 in Figures 3, 4A and 4B in the Li patent is an automatic scan test enable signal assertion system) comprising: a scan test enable signal assertion system for automatically asserting or

deasserting a scan test enable signal in response to transitions in a trigger signal (OR gate 94 in Figure 4B is a scan test enable trigger sensing component; the output of the scan test enable trigger sensing component OR gate 94 provides a scan mode signal which is a logical signal provided to place scan elements into active or inactive to trigger the scan elements, hence the scan mode signal is an assertion or deassertion notification, see Abstract in Li) and stage progression signal (a clock is a stage progression signal); a mutliplexer (MUX) coupled to said automatic scan test enable signal assertion system, said multiplexer facilitates transmission of signals depending upon the assertion of a scan test enable signal (see MUX F-Fs 62, 68, 75, 81 and 87; Note: MUX F-Fs facilitate transmission of test signals depending upon the assertion of a scan test enable signal outputted from the scan test enable trigger sensing component OR gate 94); a functional component coupled to said multiplexer, said functional component performs normal operations of an ASIC or printed circuit board (Integrated Circuit Logic 70 is a functional component for performing normal operations of an ASIC or printed circuit board); an input port coupled to said functional component, said input port functions as input connections that communicate signals to said ASIC or said printed circuit board (Pads 50 and 51 are input ports); a NAND gate coupled to said input port, said NAND gate for capturing information from said input port [OR gate 94 in Figure 4A and 4B is coupled to Pad 50 and furthermore NAND logic can be used to implement the OR logic circuit taught in Li, in fact, ((A NAND A) NAND (B NAND B)) = A OR B, hence OR logic is mathematically isomorphic to NAND logic and it would not only be obvious to use NAND logic in place of OR logic but it would be mathematically trivial]

and a test data output port coupled to said multiplexer (see 89 in figure 3 of Li). The examiner would like to point output that the circuit of Figure 3, 4A and 4B taught in Li provides a scan test enable signal activation system that allows external activation and operation of the test system during testing designed to be incorporated into a scan test system providing test data output (see 89 in figure 3 of Li) to be uploaded to the analysis component of the scan test system.

However Li, does not explicitly teach the specific use of said test data output port for communicating test data off of said ASIC or said printed circuit board from either said functional component or said input port.

Jin, in an analogous art, teaches teach the specific use of a test data output port for communicating test data off of said ASIC or said printed circuit board from either said functional component or said input port (see SO port 206 in Figure 7 of Jin) to be uploaded to the analysis component of the scan test system in the case whereby the analysis component exists external to the chip in a standard IEEE 1149.1 configuration.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Li with the teachings of Jin by including use of a test data output port for communicating test data off of said ASIC or said printed circuit board from either said functional component or said input port. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a test data output port for communicating test data off of said ASIC or said printed circuit board from either said functional component or said input port would have provided the

opportunity to communicate test data for eternal access thereby reducing circuit requirement for the IC under test.

35 U.S.C. 103(a) rejection of claim 12.

The MUX's 62 and 68 in LI serve the purpose of capturing data to be inputted into a functional logic component of an integrated circuit hence using a NAND gate in place of the MUX in Fig. 3 of Li does not deviate from the scope or the intent of the teachings in the Li patent.

35 U.S.C. 103(a) rejection of claim 13.

See Figure 3 in Li and rejections to claims 11 and 12, above.

35 U.S.C. 103(a) rejection of claim 14.

See MUX F-F 75 in Figure 3 of Li.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133
March 27, 2003

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
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